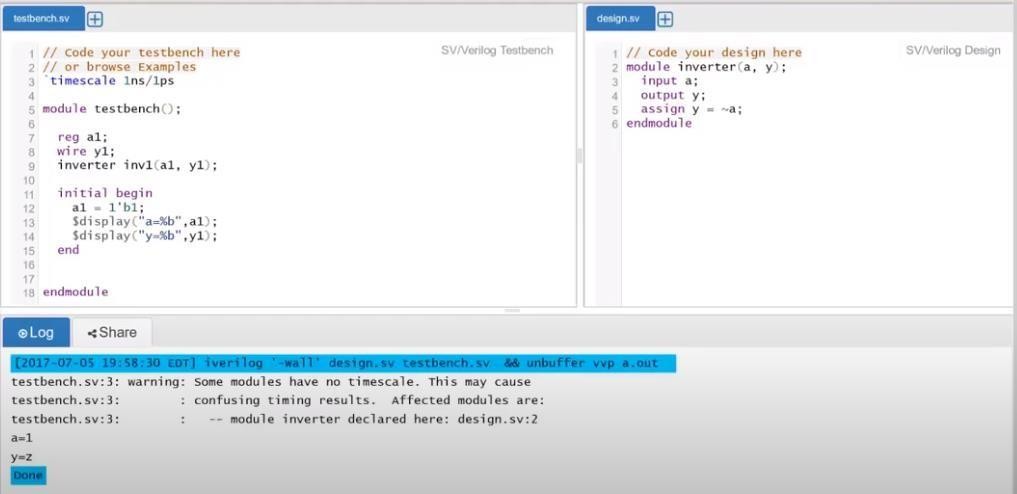
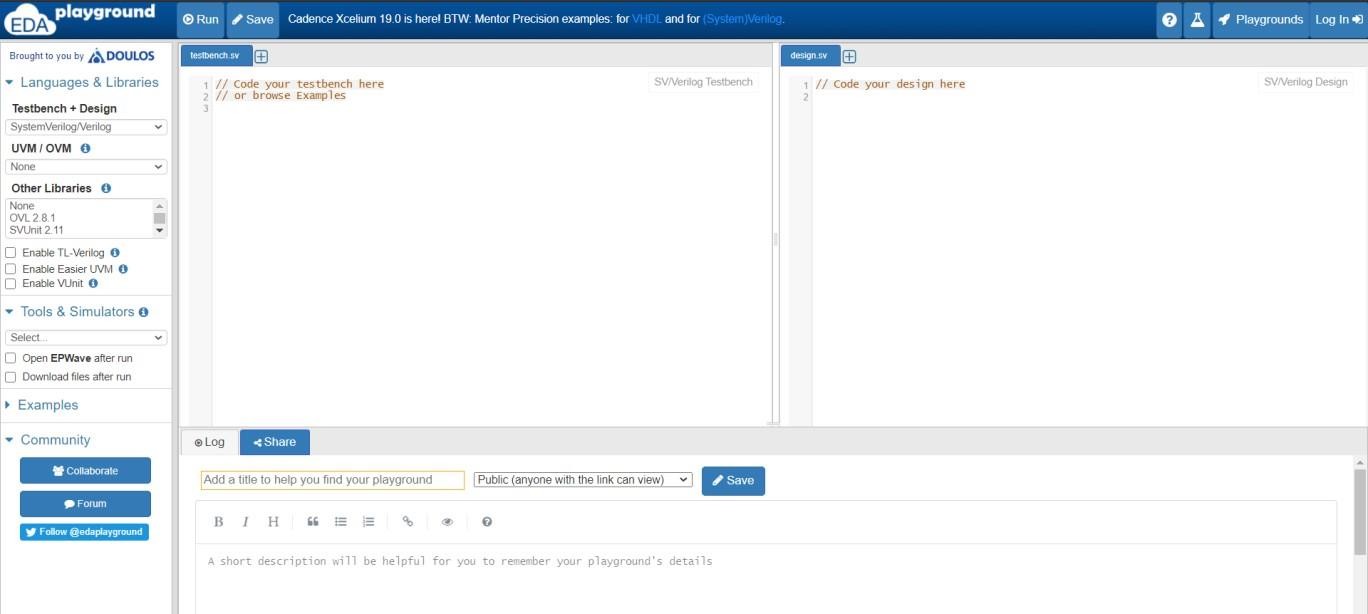
ASSESSMENT 15

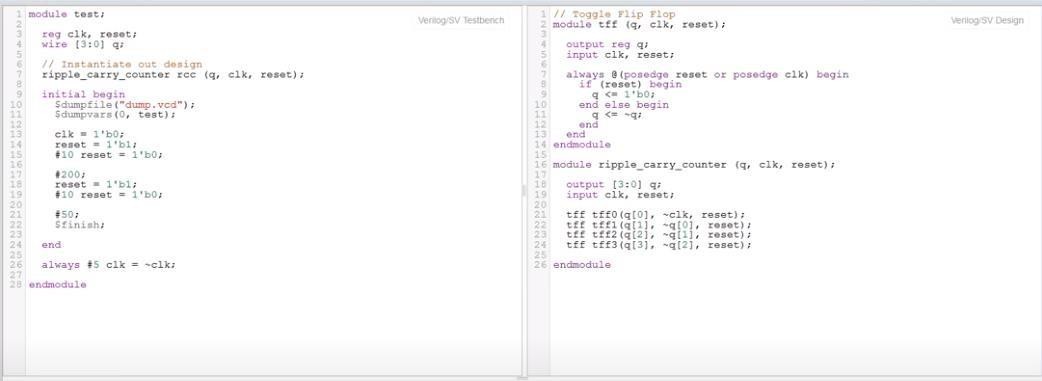
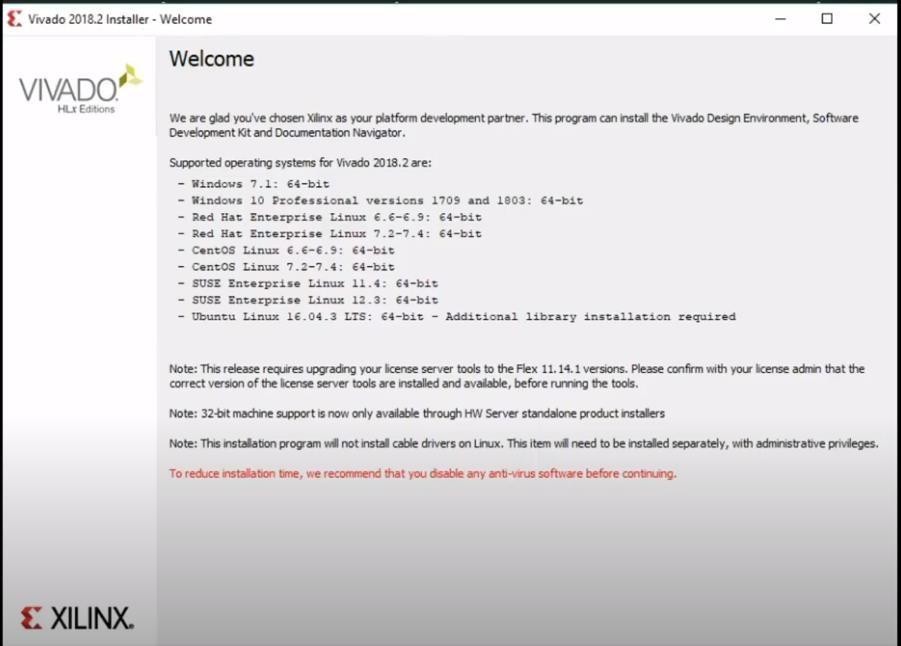
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| --- | --- | --- | --- |
| **Date:** | 03-06-2020 | **Name:** | Sheela Golasangi |
| **Course:** | DIGITAL DESIGN USING HDL | **USN:** | 4AL16EC068 |
| **Topic:** | * EDA Playground Online complier * EDA Playground Tutorial DemoVideo * How to Download And Install Xilinx VivadoDesign Suite * Vivado Design Suite for implementation of HDLcode | **Semester & Section:** | VIII  ‘B’ |
| **Github Repository:** | Sheela-Course |  |  |

|  |
| --- |
| **Image of session**    **Report**  **Vivado DesignSuite for implementation of HDL code**   1. In a separate web browser window, log in toEDA Playground 2. Log in Click the Log in button (top right) Then eitherclick on Google or Facebook or   register by clicking on ‘Register for a full account’ (which enables all the simulators on EDA Playground)   1. Select ‘Aldec Riviera Pro’ from theTools & Simulatorsmenu. This selects the Aldec Riviera Pro simulator, which can be used however you logged in. Using certain other simulators will require you to have registered for a full account. 2. In either theDesignorTestbenchwindow pane, type in the following code: 3. Module test;   4. initial  5. $display ("Hello World!");  6. end module  7. ClickRun (top left) Yes, running a simulation is as simple as that!  8. In the bottom pane, you should see realtime results as your code is being compiled and then run. A run typically takes 5seconds, depending on network traffic and simulator. Near the bottom of result output, you should see:  9. Hello World!  10. Now, let’s save our good work. Click theSharetab near in the bottom pane and then type in a name and description. Then clickSave  11. The browser page will reload and the browser address bar will change. This is a persistent link to your saved code. You can send the link by email, post it on a web page, post it onStack Overflowforums, etc.  12. Now, let’s try modifying existing code. Load the following example:RAM  13. On the left editor pane, before then do initial block, add the following:  14. write\_enable = 1;  15. data\_write = 8'h2C;  16. toggle\_clk\_write;  17. toggle\_clk\_read;  18. $display("data[%0h]: %0h",  19. address\_read, data\_read);  20. Run the sim. In the results you should see this new message:  21. data[1b]: 2c  22. Optional. ClickCopyto save a personal version of the modified RAM code, including the simulation results.  Loading Waves from EDA Playground  You can run a simulation on EDA  Playground and load the resulting waves in EPWave.  Loading Waves for SystemVerilog and Verilog Simulations  Go to your code on EDA Playground. For example:RAM Design and Test  Make sure your code contains appropriate function calls to create a \*.vcd file.  For example:  initial  begin  $dumpfile("dump.vcd");  $dumpvars(1);  end  Select a simulator and check the Open EP Wave after run checkbox. ClickRun    After the run completes, the resulting waves will load in a new EPWave window.  Loading Waves for VHDL Simulations check theOpen EPWave after run checkbox.  Specify the top entityto simulate.  ClickRun  After the run completes, the resulting waves will load in a new EPWave window. (Popups must be enabled.)  The waves for all signals in the specified top entityand any of its components will be dumped.In EPWave window, click get Signalsto select the signals to view. |



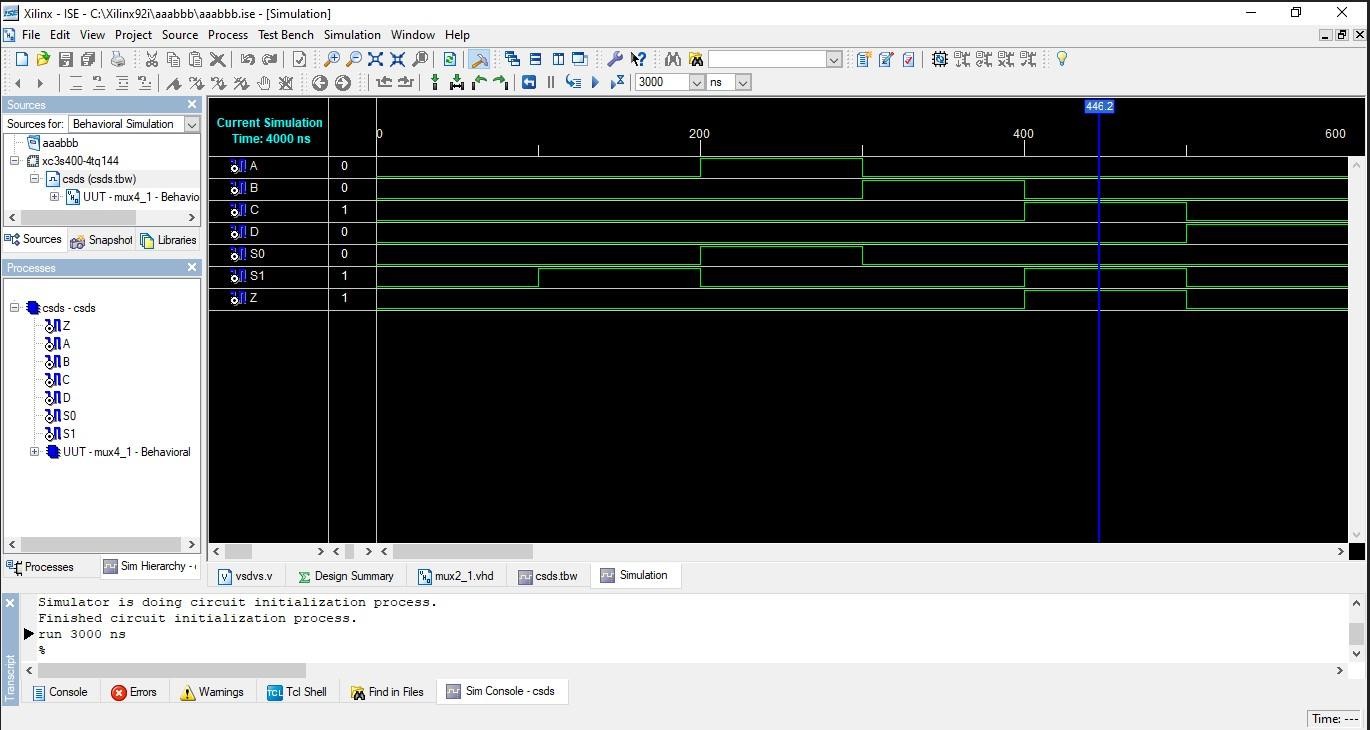
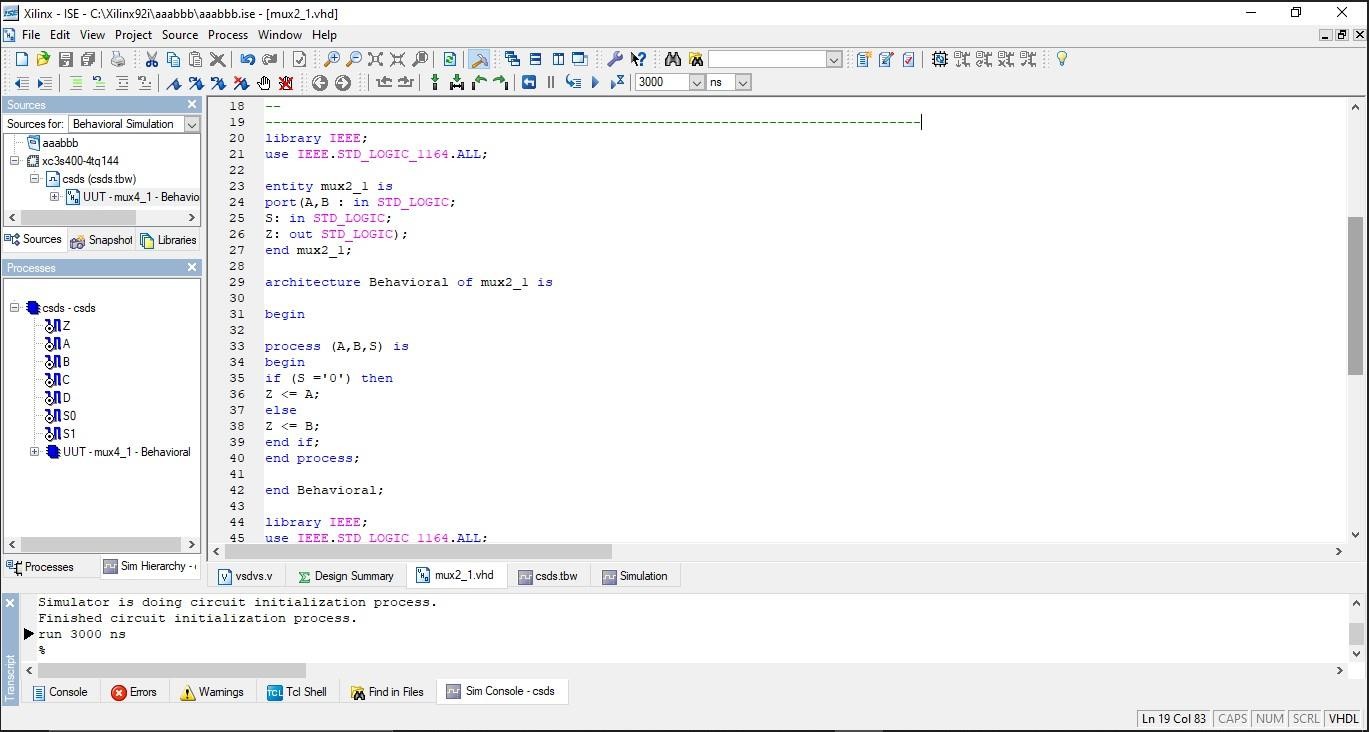
# EDA Playground Online complier:

**EDA Playground Tutorial Demo Video:**



**How to Download And Install Xilinx Vivado Design Suite:**

**Vivado Design Suite for implementation of HDL code:**



**TASK:**

Implement 4 to 1 MUX using two 2 to 1 MUX using structural modelling style and test the module in online/offline compiler.

# OUTPUT